March 14, 2005

UNITED STATES PATENT FINAL OFFICE ACTION REPLY

FOR

(TITLE):

SYSTEM AND METHOD FOR INTEGRATING A DIGITAL CORE WITH A SWITCH MODE POWER SUPPLY

APPLICANT:

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10/604,573

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2838

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REPLY TO DETAILED ACTION

Specification

The final page of this Office Action Reply includes the currently amended Abstract of the disclosure to replace in its entirety the immediate prior Abstract. The currently amended abstract has one sentence amended from the immediate prior Abstract, to comply with the formal requirement to remove the purported merits therein. The prior amended sentence that contained the phrase "highest efficiency" has been rewritten as follows: "Within the integrated circuit package including this semiconductor die also exists a switch mode DC-to-DC voltage converter, preferably a synchronous step-down regulator powering the entire integrated circuit from one supply voltage."

Claim Objections

Since the examiner's final action indicates no objections to the allowable claims, the applicant understands the prior amendments comply with all formal requirements and no further traversal is necessary for these claims.

Claim Rejections

The applicant hereby requests reconsideration of claim 1 and claim 14 as currently amended to include within the clause of "output voltage fixing circuit", the further limitation of "output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback loop."

The applicant contends that the examiner's first argument against the immediate prior amendment to these claims, "Applicant has not shown the invention in a drawing. I.e. the use of the circuit with an open-loop configuration and shows only a closed loop…", ignores multiple locations in the text of the original specification which thoroughly explicitly state the omitted portions of Figure 1 yielding the preferred embodiment of the invention disconnected from the old structure and thus adequately fulfills the requirement of 37 C.F.R. 1.83(b). Specifically, all of paragraph 20 of the original specification, repeated here for immediate reference, thoroughly and explicitly addresses the open-loop configuration in regard to features from Figure 1 needing omission in order to attain such configuration:

"The following components comprise the feedback loop common to nearly all existing step-down switch mode power supplies and therefore could constitute any implementation within the scope of the present invention although such a traditional feedback loop does not comprise the output voltage fixing circuit found in the preferred embodiment practiced within the preferred method of the present invention. All the discrete components external to the semiconductor die 100 including resistors 114, 115, 116, 118, capacitors 117, 119, 120, and substrate bonding pads 121,122, and the components internal to the semiconductor die 100 including the bonding pads 123, 124, the band-gap voltage reference 126, the reference voltage buffer 127, and the error amplifier 125 of Figure 1, and the voltage comparator 200 depicted in Figure 2 within the pulse width modulation controller 129, exist in a feedback loop in common practice of

prior art switch mode DC-to-DC converters, but this feedback loop does not exist in the output voltage fixing circuit found in the preferred embodiment practiced within the preferred method of the present invention. Nonetheless, since the circuitry of the prior art feedback loop does not constitute a substantial departure beyond the scope of the present invention, its use will hereinafter be briefly described. "

Also, Figure 3 and the text of the specification in sentences 4 through 6 of paragraph 26 provide the view of the improved portion itself while its relation to Figure 1 provides so much of the old structure as will suffice to show the connection of the old structure therein fulfilling the requirement of 37 C.F.R. 1.83(b). Here the text of sentence 4 through 6 of paragraph 26 is cited for immediate reference:

"This preferred embodiment of the pulse width or frequency modulation controller 129 achieves the significant cost-saving goal of eliminating all power supply related analog components internal to the semiconductor die 100, the voltage buffers 127, the error amplifier 125, and the analog comparator 200, through the use of what may be implemented with all digital standard cell library components. Instead of feeding back an error voltage signal through a comparator 200 to fix the output voltage 102, by characterizing the semiconductor die 100 current consumption over process variations and operating environment temperatures in all power states knowing its fixed input and output supply voltages 101, 102, values for power supply duty cycle and/or switching frequency $F_{s,}$ relative to various supply current states may be implemented in decode logic configurations, or stored in registers or memory locations as depicted by block 303

in Figure 3, and thus fix the power supply output voltage 102 precisely. The theory behind and method for implementing this innovation is described in subsequent paragraphs referencing Figure 6. "

The applicant further contends that should the examiner deem the text of the specification inadequate in portraying a view of the improved portion itself, per 37 C.F.R. 1.83(b), that a subsequent additional amendment including a new sheet per 37 C.F.R. 1.121(d) would not constitute new matter 37 C.F.R. 1.121(f). While the applicant considers a replica of Figure 1 only omitting: all the discrete components external to the semiconductor die 100 including resistors 114, 115, 116, 118, capacitors 117, 119, 120, and substrate bonding pads 121,122, and the components internal to the semiconductor die 100 including the bonding pads 123, 124, the band-gap voltage reference 126, the reference voltage buffer 127, and the error amplifier 125; a needless redundancy, if the examiner deems this necessary to fulfill the requirements of 37 C.F.R. 1.83(b), an amendment of such a new sheet could not possibly violate 37 C.F.R. 1.121(f) as new matter since this has already been thoroughly and explicitly depicted in the text of the original specification in paragraph 20.

As before, the applicant asserts this amendment does not introduce new matter under 37 C.F.R. 1.121(f) as the original specification presents digital open-loop terminology in no less than two other instances. The last sentence in the Summary of Invention introduces the open-loop configuration: "... the present invention's substantial departure from prior art and significant novelty exists in the preferred embodiment

wherein said switch mode synchronous DC-to-DC step-down converter is implemented in an open-loop configuration retaining precision based on semiconductor die power consumption characterization data...". Most precisely the original specification states this novelty of digital open-loop configuration in the last sentence of paragraph 32 in the Detailed Description describing Figure 6, "The equation in block 601 and its derivation verifies the assertion of the fundamental theoretical principle of the present invention, namely, given fixed input and output voltages 101, 102, and having characterization data defining all supply current states I_o, with empirical data or even reasonably accurate estimates stating the component losses, one may digitally fix the duty cycle of a high efficiency synchronous switch mode power supply in an open loop configuration and still obtain a precise output voltage 102 while eliminating the expense of the frequency compensated feedback loop and especially the precision analog circuits internal to the semiconductor die 100". This very sentence also clearly points out the patentable novelty over the cited reference Rozsypal (U.S. Patent 6,781,353) as well as the cited reference Ito et al. (U.S. Patent 6,683,767). Rozsypal (U.S. Patent 6,781,353) clearly states, "Error amplifier 247 is a standard analog amplifier formed in the regulation feedback path..." in line 9 of column 5, implying an analog closed-loop voltage control algorithm. Also in the invention of Rozsypal (U.S. Patent 6,781,353), comparators 220, 230, 247 and current references 242, 246 are analog components that fix the output voltage in a closed-loop configuration, the closed-loop being defined by the path from the output voltage back through the analog comparators 220, 230, 247 through the logic blocks 221, 250 which

directly control the output voltage. Likewise, Ito et al. (U.S. Patent 6,683,767) presents a plurality of analog precision components internal to the semiconductor, i.e. the reference voltage generators 60, 100, and particularly the differential amplifier 41 and reference voltage buffer 110. While Ito et al. (U.S. Patent 6,683,767) does not detail the control algorithm for precise output voltage control of the switch mode power supply, an analog reference voltage generator 110 is clearly depicted in Figures 29 and 30 for such use. Thus while the references cited preclude the present invention's claim 1 in its original broad form, the currently amended claim 1 with the further limitation of "output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback loop" best describes in broadest form the patentable novelty over the references cited.

Furthermore, the references of Herbert (U.S. Patent 5,132,606) and Rozsypal (U.S. Patent 6,781,353) cited in the examiner's final action of rejecting claim 1 and claim 14 both rely upon a feed forward control algorithm. The present argument by the applicant will make no attempt to interpret or to speculate the meaning in the phrase "essentially open loop control" in Herbert's sentence "Feed forward control is essentially open loop control." But by strictest topological definition it is obvious that feed forward control forms a closed loop in its connection to the associated process blocks and thus fundamentally differs from true open-loop control where no such closed loops exist. In the Herbert U.S. patent 5,132,606 Figure 1 function blocks 3, 5, 7, and 9 comprise the feed-forward connections forming a closed loop, Figure 2 function blocks 31, 37, 39, 47,

and 27 comprise the feed-forward connections forming a closed loop, Figure 4 function blocks 65, 75 and 67 comprise the feed-forward connections forming a closed loop, Figure 11 function blocks 223, 237, 235, 225, comprise the feed-forward connection forming a closed loop, and Figure 12 function blocks 253, 269, 267, 265, and 255 comprise the feed forward connections forming a closed loop. But most pertinent to the examiner's argument, no figure illustrates the Herbert invention comprising a control algorithm of true open loop topology. The Rozsypal U.S. patent 6,781,353 likewise unequivocally lacks this obvious fundamental topological feature in all of its drawing figures. Nevertheless, because Herbert's aforementioned "essentially open loop control" sentence set a precedent of ambiguity, to avoid future misinterpretation as such, the current amendment offers in no uncertain terms the differentiating change of "a digital open-loop output voltage fixing circuit" to "an output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback loop."

Finally, noting that the specification of the present invention explicitly states in the text the removal of the circuits comprising the feedback closed loop and nowhere indicates any need for a feed-forward closed loop in the topology of the circuit, this renders the present invention patentable over the cited references.

The applicant hereby requests reconsideration of claim 14 in its currently amended form. Once again, the further limitation of the clause: "output voltage fixing circuit comprising digital open-loop means requiring no feed-forward loop and no feedback

loop" renders this currently amended claim 14 patentable over the references cited based on the same argument for reconsidering the currently amended claim 1.

Allowable Subject Matter

As claims 4-13 and 15-21 have been deemed allowable according the examiner's final action, the applicant understands the prior amendments comply with all formal requirements and no further traversal is necessary for these claims.

Conclusion

With this response to the final office action came an amendment of claims and new arguments with a Request for Continued Examination under 37 C.F.R.114(c). Therefore, the applicant concurrent to this facsimile transmittal has paid the fee defined in 37 C.F.R 1.17(e) for a small entity defined by 37 C.F.R. 1.27(a) for the Request for Continued Examination. If the currently amended claims are deemed allowable without the need for Continued Examination, please inform all necessary parties of a refund of the Request for Continued Examination fee. Since the examiner has indicated allowable subject matter, the applicant may subsequently request an international-type search report under 37 C.F.R. 1.104(a)(4). The applicant can be reached at (949) 457-0751 from 9am-10:30 am EDT Monday through Friday, or else a voice mail or facsimile message may be left at that telephone number at any time. The applicant's email address is: gizara@cox.net and is a preferred means of communication.

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Signature

Today's transmission shall be deemed authentic per 37 C.F.R. 1.4(d) by virtue of the signature hereunder of Andrew R. Gizara, the sole inventor and applicant.

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Andrew R. Gizara Sole Inventor and applicant
3/14/2005